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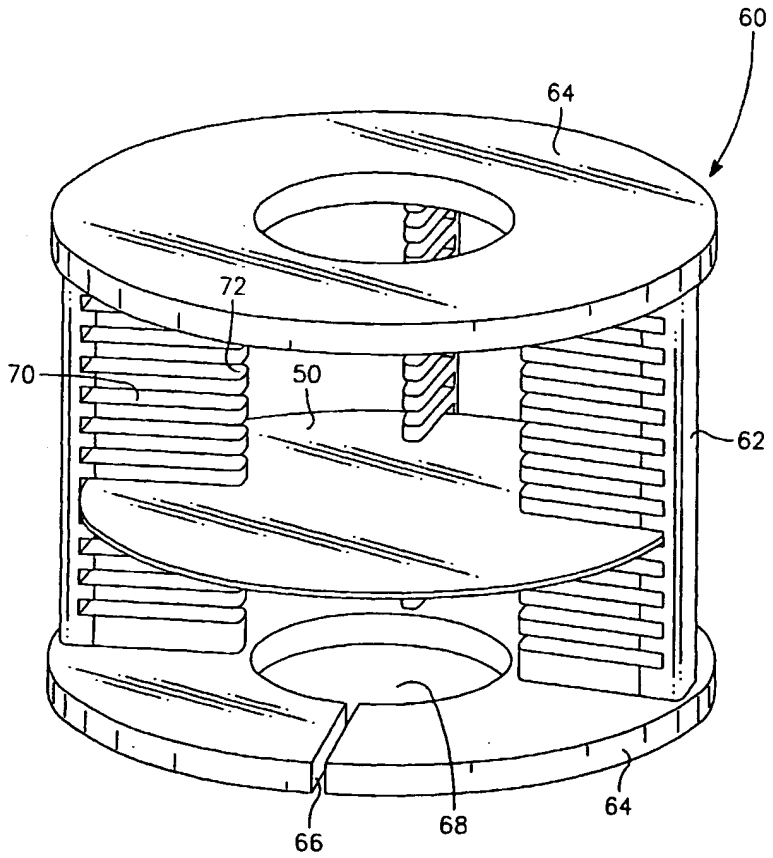
(54) Title: SILICON FIXTURES USEFUL FOR HIGH TEMPERATURE WAFER PROCESSING



(57) Abstract: A silicon-based wafer support tower (60) particularly useful for batch-mode thermal chemical vapor deposition and other high-temperature processes, especially reflow of silicate glass at above 1200°C. The surfaces of the silicon tower are bead blasted to introduce sub-surface damage, which produces pits (20) and cracks (22) in the surface, which anchor subsequently deposited layer (32) of, for example, silicon nitride, thereby inhibiting peeling of the nitride film. The tower parts are preferably pre-coated with silicon nitride or polysilicon prior to chemical vapor deposition of these materials, or with silicon nitride prior to reflow of silica. The surface roughness may be in the range of 0.25 to 2.5μm. Wafer support portions (72) of the tower are preferably composed of virgin polysilicon. The invention can be applied to other silicon parts in a deposition or other substrate processing reactor, such as tubular sleeves and reactor walls (82). Tubular silicon members are advantageously formed by extrusion from a silicon melt or by fixing together silicon staves (94) in a barrel shape (100).

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Silicon Fixtures
Useful for High Temperature Wafer Processing

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates generally to semiconductor processing. In particular, the invention relates to wafer support fixtures and reactor tubes used in batch-mode processing such as chemical vapor deposition and high temperature annealing.

2. Background Art

The fabrication of silicon integrated circuits typically involves one or more steps of chemical vapor deposition (CVD). Many advanced deposition processes use plasma enhanced CVD to activate the chemical reaction resulting in the deposition of the film from a precursor gas. The plasma process allows low temperature deposition. On the other hand, thermal CVD is performed at elevated temperatures to thermally activate the chemical reaction resulting in the deposition of the film from a precursor gas. The temperatures associated with thermal CVD tend to be much higher than those for plasma enhanced CVD, but thermal CVD temperatures fall within a wide range depending upon the material being deposited and the precursor gas.

Thermal CVD is typically utilized for the deposition of silicon nitride and polysilicon. The silicon nitride is used, for example, for etch stop layers and anti-reflective coatings. Silicon nitride has a nominal composition of Si_3N_4, but some compositional variation is expected, such as SiN_x, where x ranges between 1.0 and 1.5. Polysilicon is polycrystalline silicon. It is used for anti-reflective coating and, when doped, for interconnects and electrodes.

Despite the trend to single-wafer processing chambers, batch processing for thermal CVD continues to be widely practiced because of its high throughput and the relatively low cost of equipment. Furthermore, thermal CVD can produce highly uniform films in batch processing. In batch CVD processing, a large number of silicon wafers are loaded onto a support fixture that is placed into a thermal CVD reactor. Typically, the support fixture is a

tower in which the multiple wafers are supported horizontally and spaced vertically apart. Some applications continue to use boats as support fixture in which the multiple wafers are supported substantially vertically and spaced horizontally apart.

In the case of the deposition of silicon nitride, the precursor gas is typically composed of a silane or a chlorosilane and a nitrogen source such ammonia. At elevated temperatures, typically in the range of 600 to 800°C but sometimes extending down to 400°C or even lower, the precursors react near the surface of the wafer to deposit silicon nitride on the wafer surface. In the case of chlorosilane and ammonia precursors, the reaction products are Si_3N_4 and NH_4Cl. The former deposits on the wafer while the latter is volatile and is evacuated from the furnace. However, thermal CVD tends to coat all surfaces exposed in the furnace. In particular, the support tower is typically coated with as much silicon nitride as is the wafer. Further, the walls of the reactor, typically formed in a tubular shape, also tend to be coated.

Quartz has in the past been the most prevalently used material for support towers and tubes used in a thermal CVD process and other high-temperature processes. Quartz has a chemical composition of amorphous silicon dioxide, which is compatible with most silicon processing. At the relatively low temperatures usually experienced in CVD, whether thermal or plasma enhanced, quartz remains in a glassy state with a very smooth surface so that it is a very clean material. However, as the feature sizes on integrated circuits has decreased to 0.18μm and even smaller, quartz support towers have nonetheless experienced substantial problems because of their tendency to produce particles. These particulates fall on the wafer and can significantly reduce the yield of operable integrated circuit dies obtained from the wafer.

Often integrated circuit fabrication is monitored by measuring the number of particles added to a wafer by any step of the fabrication process. It has been found in thermal CVD of silicon nitride that the number of particles generally increases with the number of runs or batches that the quartz tower has processed. As illustrated in FIG. 1, a new tower produces relatively few particles. Thereafter, the number of particles increases with the number of runs, but up to about forty runs the number is acceptable, though still somewhat high. However, after some number of runs, the number of particles greatly increases to a totally unacceptable level. It is believed that the origin of the problem is that the silicon nitride is also depositing on the quartz tower. For 40 runs of depositing 0.15μm

of silicon nitride, a typical nitride layer thickness in an integrated circuit, the nitride may build up on the tower to a thickness of 6μm. Silicon nitride has a coefficient of thermal expansion that is significantly different than that of quartz, about 3×10^{-6} versus 0.5×10^{-6}/°C, and the nitride does not bond well with the glassy quartz surface. Differential thermal expansion between the two materials as the tower is cycled between room temperature and the relatively modest thermal CVD temperatures causes the thickly deposited nitride to peel from the quartz and to produce nitride particles, some of which settle on the wafers.

For these reasons, it is typical practice in a production environment to use a tower only for a predetermined number of runs somewhat below the experimentally determined point at which the particle count rapidly increases, for example, thirty runs for the data displayed in FIG. 1. It is common practice to then clean the quartz tower in bath of hydrofluoric acid and nitric acid to remove the silicon nitride and to return the cleaned tower to service for another cycle of runs. However, the baseline particle count for a cleaned tower is somewhat higher than that for a new tower, and the number of runs before onset of unacceptable particle count is reduced by about 25%. As a result, quartz towers are typically discarded after only two or three cycles. Although quartz towers are relatively inexpensive, such short life greatly increases the cost of ownership (COO) when measured per wafer. Also, the necessity of changing out towers and cleaning towers complicates the work flow and reduces productivity.

Furthermore, the baseline particle counts for quartz towers are still high, and the onset of greatly increased counts is somewhat variable. Both factors reduce the yield of operable dice obtained from the wafers.

Quartz tubes are also often replaced after a finite number of batches although the problem being addressed is often fracturing of the quartz tube.

Some of these reasons have prompted the use of silicon carbide towers. Bulk silicon carbide is typically formed by a sintering process, which produces a material containing a high fraction of impurities. For this reason, the sintered material is usually covered with a layer of CVD silicon carbide. As long as the CVD layer is not punctured, contamination is not a problem. The peeling problem is not totally eliminated. However, after a nitride buildup of about 20μm on the silicon carbide tower, it can cleaned in a mixed acid etch for up to a week with the result that the tower can be used almost indefinitely. However, the CVD silicon carbide film is fragile, and a single pin hole through the film ruins the

protective coating resulting in the necessity that the tower be scrapped. Entire towers of CVD silicon carbide can be made, but they are very expensive.

Accordingly, it is greatly desired to provide a support tower that is not subject to such particle problems and can be used for many more runs without cleaning or replacement.

Suggestions have been made to form wafer support towers from silicon, particularly polysilicon. See, for example, US Patent 6,056,123 to Niemirowski et al. They fabricate their towers from silicon legs mechanically wedged into silicon end plates, and a layer of polysilicon is then deposited by chemical vapor deposition on the assembled structure to provide additional strength. Their tower fabrication is believed to still be weak. Further, when silicon towers are used to support wafer preformed with a silica glass that requires reflowing at high temperature, the wafers have been observed to stick to the tower after reflow. Forcefully removing the stuck wafer may result in the tower becoming chipped. Some believe that the silica glass reflows over the edge of the wafer and intimately bonds with the exposed silicon and a silica bridge is formed between the wafer and the tower.

SUMMARY OF THE INVENTION

The invention includes a method of chemical vapor deposition (CVD), particularly thermal CVD, and more particularly deposition of silicon nitride, polysilicon, and related materials, onto multiple wafers supported on a silicon fixture, for example, a tower. Preferably, the silicon fixture is composed of virgin polysilicon. Also, preferably, surfaces of the silicon tower are subjected to surface treatment, such as bead blasting by hard particles, for example, of silicon carbide. The surface treatment may be characterized as introducing sub-surface damage in the silicon part.

The invention also includes such a silicon fixture and its fabrication method. The surface of the fixture has a roughness preferably in the range of 10-100 microinches Ra (0.25-2.5μm), more preferably 20-75 microinches Ra (0.5-1.9μm), and most preferably 30- or 35-50 microinches Ra (0.75- or 0.9-1.25μm).

The invention further includes other surface treated silicon parts usable in a CVD reactor or other high-temperature substrate processing reactor.

According to another aspect of the invention, a silicon tower is pre-coated with a thin layer, for example, by chemical vapor deposition. When the tower is supporting wafers

in high-temperature deposition of silicon nitride or polysilicon, the tower is preferably initially pre-coated with a thin layer of silicon nitride or polysilicon respectively. Cracks and pits produced the surface treatment firmly anchors the initial film and subsequently deposited films. When the tower is supporting wafers in high-temperature deposition or oxidation producing silica, the tower is preferably initially coated with a thin layer of silicon nitride.

The invention is further applicable to a high-temperature reflow step following deposition of silica layer, for example, by CVD or flame hydrolysis. The reflow step is typically performs at above 1200°C, preferably at 1350±30°C for a commonly used silica formulation, and most preferably at 1360±10°C .

In a further aspect of the invention, silicon tubular members may advantageously be used for liners in CVD reactors and for tubular reactor walls used in high-temperature processing. Such silicon tubular members may conveniently be formed by extrusion, whether or not the tube is surface treated, or by bonding together in a polygonal shape a large number of trapezoidally shaped staves and preferably thereafter machining the interior to form a cylindrical bore. Such silicon tubes are often advantageously surface treated and pre-coated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic chart showing the generation of particles during batch thermal chemical vapor deposition using a quartz tower of the prior art.

FIG. 2 is an orthographic view of a silicon tower fabricated according to the invention and usable in the processes of the invention.

FIG. 3 is a cross-sectional view of a surface of the silicon tower after bead blasting.

FIG. 4 is a cross-sectional view of the silicon tower surface of FIG. 3 after deposition of a pre-coat layer.

FIG. 5 is a cross-sectional view of the silicon tower surface of FIG. 4 after many runs of depositing silicon nitride.

FIG. 6 is a schematic cross-sectional view of a thermal CVD reactor in which a process of the invention may be practiced and in which the tower or shield of the invention may be used.

FIG. 7 is an orthographic view of another silicon tower usable with a high-

temperature reflow process.

FIG. 8 is a schematic orthographic view of a tubular reactor having silicon sidewalls.

FIGS. 9 is a cross-sectional view illustrating the fabrication of a silicon tube by fixing together a plurality of horizontally extending silicon staves.

FIG. 10 is a cross-sectional view of staves having a tongue-and-groove structure.

FIG. 11 is a cross-sectional view of a circularized silicon tube.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

Silicon fixtures, particularly horizontally extending boats, have been frequently suggested and occasionally used in the past. However, their assembly has presented sufficient problems to prevent the widespread use of silicon towers. Many of these problems with silicon support fixtures have been addressed in a set of patents, U.S. Patents 6,196,211, 6,205,993, and 6,225,594 to various of Zehavi, Davis, and Delaney. Boyle et al. in U.S. Patent Application, Serial No. 09/608,557, filed June 30, 2000, published as International Publication Number WO 02/03428 A3 and incorporated herein by reference in its entirety, disclose in detail a method of fabricating one embodiment of such a silicon tower 10, illustrated in FIG. 2. The tower 10 includes multiple silicon legs 12 joined at opposed ends to silicon bases 14. Teeth 16 are cut into the legs 12 to support the wafers.

It is preferred that at least the legs 12 are composed of virgin polysilicon (virgin poly) formed from the chemical vapor deposition of silane or chlorosilane. Such a material is virtually free of contaminants, particularly the rapidly diffusing metals so deleterious to silicon integrated circuits. The bases may be formed of Czochralski (CZ) silicon, preferably polysilicon although monocrystalline may be used, since virgin poly is not typically available in such large diameters. Other forms of silicon such as cast silicon may be used. The process includes joining the legs 12 to the bases 14 with a spin-on glass (SOG) or other glass-like compound followed by high-temperature ambient annealing at preferably between 1025 and 1400°C to vitrify the SOG and bond it to the already oxidized silicon parts. Alternatively, the pieces may be laser welded together in a process described by Zehavi et al. in US Patent 6,284,997, incorporated herein by reference in its entirety. The advantage of either method is forming a continuous planar bond extending along the plane of the interface between the two fixed pieces, unlike the mechanical wedges and surface layer of Niemirowski et al.

After assembly, the tower 10, including both the legs 12 and bases 14, is subjected to a surface treatment to introduce controlled sub-surface damage in the silicon. Such a surface treatment virtually eliminates the particle problem usually associated with thermal CVD of silicon nitride. We believe that the surface treatment not only removes the thick oxide layer formed in the SOG anneal, but also, as illustrated in the cross-sectional view of FIG. 2 produces pits 20 and cracks 22 penetrating into the treated surface 24 of the silicon part 26 of the tower 10. The silicon part 26 may be one of the legs 12 or one of the bases 14.

When the tower enters service, it is preferably first subjected to a pre-treatment similar to a typical nitride CVD deposition in which a silicon nitride pre-coat layer 28 not only covers the part surface 24 but also fills the pits 20 and cracks 22 to produce a smooth pre-coat surface 30. Typical thicknesses of the pre-coat layer 28 range between 0.1 and 10μm. Preferably, during the pre-treatment, no wafers are inserted in the tower slots to be used in production. The silicon nitride in the pits 20 and cracks 22 firmly anchors the pre-coat layer 28 to the silicon part. Thereafter, when the tower enters normal production, subsequently deposited silicon nitride layers 32 are sequentially deposited over the silicon nitride pre-coat layer 28, which is firmly anchored to the silicon part 26. Although differential thermal expansion continues to exist between the nitride layers 32 and the underlying bulk silicon 26, the force exerted at the interface is insufficient to peel the nitride layers 32 from the part 26.

An effective method of work treating the silicon surface is to roughen it by bead blasting, which is similar to industrial sand blasting. A preferred such method is to blast the surface with particles of silicon carbide of 220 grey grit in a Model 48/PP dry blaster available from Trinity Tool Co. of Fraser, Michigan. Particle velocity is controlled by an exit pressure of between about 20 and 80psi. In the bead blasting, the blasting wand is manually swept over all exposed surfaces of the assembled tower. The blasting need not visibly roughen the silicon surface. The silicon surface following the preceding high-temperature SOG anneal has a bluish color, arising from the thick surface oxidation. The blasting is continued until the bluish color turns gray, indicative of silicon with perhaps a very thin native oxide. Preferably, the silicon carbide particles are relatively pure to above 99%, particularly with respect to metals. Use of particles with significant metal contaminants will likely introduce the metal into the silicon part, rendering the treated part

much less useful for processing silicon integrated circuits.

Following bead blasting, the treated silicon surface is cleaned by vigorous washing with a biodegradable, non-phosphate detergent such as Escolex to remove silicon particles clinging to the surface. A final clean with a high-pressure carbon dioxide gun, such as Sno Blo, removes any remaining particles. The final surface roughness has been measured to be typically about 32 microinches (0.8μm) on the virgin poly legs and 50 microinches (1.3μm) on the CZ bases. A preferred range of surface roughness, particularly for the legs, is 10 to 100 microinches Ra (0.25 to 2.5μm Ra). A more preferred range is 20-75 microinches Ra (0.5-1.9μm Ra), and a most preferred range is 30- or 35-50 microinches Ra (0.75- or 0.90-1.25μm Ra).

It is preferred that no post-treatment etching be performed as this would likely remove the pits and cracks. Post-treatment polishing is also not preferred, except possibly in the wafer bearing surfaces which, in a preferred embodiment, are cut into teeth slanting upwards from the legs at 1 to 3° from the horizontal.

Other hard particles may be used for the blasting, such as ceramics. However, the material must be substantially free of metals known to readily diffuse in silicon and affect its semiconductor qualities. Other types of surface treatment are possible, such as lapping and grinding. However, these processes are dirty, and offer no apparent advantage.

The silicon tower 10 fabricated according to the above process is used in a batch CVD reactor 40, as illustrated in FIG. 6, which is heated by a resistive coil 42. The reactor is supplied with precursor gases including silane or a chlorosilane such as $SiClH_3$ and ammonia (NH_3) from source 44, 46, and a vacuum (exhaust) pump 48 evacuates reactants from the interior of the reactor 40. The pump 48 may maintain the interior of the reactor 40 at anywhere in the range from approximately atmospheric pressure for atmospheric pressure CVD (APCDV) down to about 10 Torr for low pressure CVD (LPCVD). Multiple wafers 50 are loaded into the tower 10 and processed as described above to deposit the silicon nitride in one batch run. When a boat instead of a tower is used, the thermal CVD reactor is typically in the form of a horizontally extending tube, into which the boat bearing multiple wafers is horizontally inserted. The same production reactor may be used to pre-coat the silicon nitride layer onto the tower while no wafers are supported in production slots.

Nitride pre-coats are believed to provide increased surface integrity of the silicon parts in a hot or harsh environment because of the known toughness of silicon nitride.

Such surface-treated silicon towers can be used for hundreds to thousands of runs. The nitride build up seems to be limited only by the accumulating nitride filling the slots between the teeth and impeding mechanical clearance of the wafers. Such thicknesses of silicon nitride can be removed by reslotting the teeth or by a long etch in hot hydrofluoric acid.

Polysilicon is also frequently deposited by thermal CVD typically using a silane or chlorosilane precursor gas. A silicon tower for polysilicon CVD deposition is advantageous since the CVD polysilicon is well matched to the virgin poly and possibly other forms of silicon in the tower. A smooth silicon tower surface may suffice for polysilicon deposition. However, it has been observed that CVD polysilicon flakes from IC wafers. Accordingly, if the same mechanism applies to silicon towers, the surface treatment of the invention is useful in providing additional bonding between the bulk silicon parts and the deposited polysilicon layers.

The silicon tower subjected to the nitride pre-coating described above can be used in a very high temperature anneal step, such as a reflow of a silicate glass. Thick layers of silicate glasses may be formed by flame hydrolysis deposition (FHD) in which silane is supplied to a hydrogen and oxygen torch and the flame is passed over the substrate, typically a silicon wafer, to deposit a silicate glass having a nominal composition of SiO_2. Germane or other germanium precursors may be additionally included in the flame feed, as well as is water vapor, to affect the refractive index and dielectric constant of the deposited glass. However, the so deposited material is typically not homogeneous and requires for a commercially popular formulation of the silicate glass a high-temperature reflow at 1350°C±30°C, preferably 1360°C±10°C typically in an air ambient, to convert the material to a homogeneous glass. Some other types of glasses reflow at as low as 600°C, but the problems described below tend to become problems only at reflow annealing temperatures of greater than 1200°C. A silicon tower is sufficient for supporting substrates in such a high-temperature process since it remains relatively strong close to its melting point of 1416°C.

One such silicon tower 60, illustrated in the orthographic view of FIG. 6, was designed for such a high-temperature process. The tower 60 has three silicon legs 62, preferably of virgin polysilicon, joined to two silicon bases 64 with a radial expansion slot 66 formed in the lower one between its outer periphery and an inner aperture 68. Each leg

62 includes multiple teeth 70 upwardly inclined at angles of between 86° and 89° with respect to the longitudinal axis of the leg 62 with a support surface 72 formed substantially perpendicularly to the longitudinal axis for supporting one of multiple wafers 50. The support surfaces 72 may be polished to a mirror smoothness. In order to minimize wafer droop at the very high processing temperatures, it is preferred that the legs 62 be located at about 120° angular spacings with long teeth 70 having their support surfaces 72 located at about 0.707 of the wafer radius although a position at between 69% and 72% of the wafer radius would provide nearly equal results. Droop can be further reduced by the use of four legs with their support surfaces arranged in a square pattern at 0.707 of the wafer radius.

However, at the temperatures required for reflow, the silicate glass tends to drip over the edge of the wafer and to contact the support tower around the edges of the wafer. If the contacted material is silicon, the very hot silicate glass is likely to chemically bond to the silicon. After completion of the reflow when the temperature is reduced, the wafer is believed to be bonded through the reflowed glass to the tower. Excessive force in breaking the bond may chip the silicon of the tower or fracture the wafer, either creating major contamination problems.

The chipping and fracturing can be greatly reduced if the assembled silicon tower before use is pre-coated with of a layer of silicon nitride to a thickness in the range of 0.1 to 10μm, 0.3μm being a typical minimum thickness. The deposition onto all areas of the tower used to support production wafer may be performed by chemical vapor deposition, as described above. Nitride tends not to wet other materials such as silica and silicate glasses and the nitride does not react with silica so that the reflowed glass contacting the nitride pre-coat is easily released and removed from the processing chamber with the wafer. Wafers annealed on such a nitride pre-coated tower have been observed to less readily stick to the tower and to not be chipped. Although it is recommended that the silicon tower be surface treated prior to the nitride pre-coating, in this application, nitride flaking is much less of a problem so that the surface roughening provided by surface treatment may not be needed. However, the surface roughness produced by the surface treatment increases the adhesion of the nitride pre-coat layer to the silicon tower and thus further prevents peeling of nitride when the reflowed glass is forcefully removed. Thereby, the integrity of the nitride pre-coat layer is preserved over a long commercial use.

The same preventive mechanism is useful when the wafer is being flame hydrolyzed

while supported on a silicon pedestal fixture pre-coated with a nitride layer.

Although the invention is particularly useful for support towers and boats supporting multiple wafers, it may also be applied to other parts that are exposed to deposition. For example, a tubular sleeve 76 may be inserted in the CVD reactor 40 of FIG. 6 to control the flow of gases in the reactor. Whatever deposition occurs also coats the interior of the sleeve 76, which may be removed and replaced. In the past, the sleeve 76 has been composed of quartz. A quartz sleeve suffers many of the same problems as a quartz tower. Instead, according to the invention, the sleeve 76 is composed of silicon having a tubularly shaped wall of about 2 to 5mm thickness. At least its interior walls are surface treated by bead blasting or the like to provide a good anchor for the deposition of many layers of silicon nitride. The lifetime of the treated silicon sleeve 76 is substantially longer than that of a quartz sleeve.

A silicon chamber part shaped similarly to the silicon sleeve 76 is a silicon reactor tube 80 illustrated in the schematic orthographic view of FIG. 7. It has a circularly symmetric wall 82 of thickness t enclosing a bore 84 of diameter D. A resistive heater 86 is wrapped around the tube 80 and is powered by a power supply 88 to heat the interior of the reactor to elevated temperatures. Other forms of heating are possible, such as radiant or RF inductive heating. If the silicon tube 80 has sufficiently high doping so as to be highly conductive, the RF energy may be coupled directly into the tube 80, in which case the power supply 88 supplies RF power rather than AC or DC and the wire 86 may be offset from the tube wall 82.

The diameter D is large enough to accommodate a wafer tower or wafer boat supporting a number of wafers. That is, the diameter D is somewhat larger than the wafer diameter of, for example, 200 or 300mm. For a tower, the tube is arranged vertically; for a boat, the tube is arranged horizontally and preferably the boat is support on rails cantilevered parallel to the tube wall 82. In either case, the support fixture loaded with wafers is placed in the reactor tube. In a vertically arranged reactor, either the tube is lowered over a stationary tower or the tower may be inserted vertically into a stationary tube. On the other hand, a wafer boat is moved horizontally into a stationary horizontally arranged reactor tube.

The silicon tube 80 is held between unillustrated end caps, preferably formed of surface-treated silicon, providing a support for the tower or boat and ports for the supply

gases and exhaust or vacuum pump of FIG. 6. If necessary, the end caps are vacuum sealed to the tube 80 for the relatively modest vacuums required. The thickness of the tube wall 82 is preferably at least 3mm and more preferably at least 5mm. Such a reactor tube thereby allows a large portion of the exposed surfaces of the reactor to be composed of high-purity silicon. Such reactor tubes, previously made of quartz or sometimes silicon carbide, are used for thermal CVD of silicon nitride and polysilicon, as previously described, for wet or dry thermal oxidation of silicon, for diffusion doping from an ambient including the doping material, inert annealing including a dopant drive-in, and for other high temperature processes. Advantageously, especially for thermal CVD, the interior surface of the tube wall 84 is surface treated to provide additional adhesion to the deposition material.

Other parts in this or other deposition chambers, such as pedestals, pedestal rings, and rails, typically formed of quartz in the past, may instead be formed of silicon, preferably virgin poly if it is available in adequate sizes, and thereafter surface treated as described above.

Although virgin poly is particularly advantageous for silicon parts which contact the wafer, other chamber parts such as the above described sleeve and wall do not require the very high purity levels associated with virgin poly. The surface treatment described above may be applied to other forms of silicon, for example, float zone (FZ) silicon, CZ silicon, cast silicon, edge film grown (EFG) silicon, the last two forms of which are prevalently used for solar cells, or other types such as extruded silicon. It is also possible to perform the described surface treatment on a silicon film deposited on another base material, for example, by CVD.

At the present time, virgin polysilicon is not available in diameters greater than 200mm required for the sleeve and reactor tube described above. Silicon of lesser purity is acceptable in many processing applications in which a high-temperature silicon part does not touch the silicon wafer. Nonetheless, the silicon parts should be made of silicon that is substantially pure, for example, has a impurity atomic fraction of metals of less than one part per million and of other components including oxygen, nitrogen, and carbon of substantially less than 1% and preferably less than 50 parts per million. Alternatively, the silicon may be characterized as being semiconductive.

One method of forming the tubular silicon sleeve and wall described above is extrusion of silicon in a circularly symmetric tubular shape in a process also called edge

film growth (EFG). Some older technology for doctor-blade extrusion of silicon is disclosed by Grabmaier et al. in U.S. Patents 4,330,358 and 4,357,201. This technology sinters the extruded form and uses germanium sintering aids, including semiconductor dopants if desired. More recent technology including extruding silicon tubes is disclosed by Stormont et al. in U.S. Patent 4,440,728 and by Harvey et al. in U.S. Patent 5,102,494. GT Equipment Technologies, Inc. of Nashua, New Hampshire has commercialized and markets technology for extruding large hollow silicon members in polygonal shapes, and sells an extruder under the trade name GIi EFG Puller. It has long been known to form small-diameter sapphire circular and polygonal tubes by EFG.

Silicon chamber walls may alternatively be formed by bonding together a relatively small number of silicon plates in a closed pattern as one would assemble staves into a barrel. However, this technique is not always successful because the polygonal shape may introduce non-uniform flow patterns. Further, the bonding agent used to fix the plates together may be a contaminant for semiconductor processing.

An improvement of the stave approach is illustrated in the cross-sectional view of FIG. 9. A large number of staves 90 are machined to have a cross-sectional shape of symmetric trapezoids with two parallel faces 92, 94 and two faces 96 inclined with respect to each other at angles so that the faces 96 of neighboring staves 90 are parallel. The shape uniformly extends along an axial direction. The staves 90 are composed of silicon, preferably virgin polysilicon The machining of virgin polysilicon is described in the afore cited International Publication Number WO 02/03428 A3. The staves 90 number at least twelve and preferably twenty or more. Other shapes are possible, but the symmetric trapezoid is preferred to ease machining and assembly.

The staves 90 are assembled in a closed pattern with their longitudinal axes oriented parallel to a central axis 98 with the inclined sides 96 of neighboring staves 90 abutting each other to form a tightly fitting polygonal tube 100 formed in a generally circular pattern about the central axis 98. The large number of staves reduces the interior asymmetry of the assembled tube and simplifies any circularizing. The staves 90 can be held together prior to being bonded together by sleeves or hoops of quartz or other material placed around their ends. The staves 90 are then fixed together to form a wall. For a tubular silicon liner used within another tube, the silicon tube need not be vacuum tight. However, for a silicon vacuum wall, the joints must be made vacuum tight.

The fixing process may include applying a thinned spin-on silica glass (SOG) to the inclined faces 96 before assembling the staves 90 and thereafter curing the spin-on glass, as described in previously cited International Publication Number WO 02/03428 A3. While this method is effective for tubes used at lower processing temperatures, the method suffers at very high processing temperatures because the silica glass softens at elevated temperatures. Instead, it is preferred to use a silicon welding technique described by Zehavi et al. in US Patent 6,284,997. For a non-vacuum wall, the staves 90 may be spot welded at their ends or at occasional spots along their length, and the clean silicon weld described in US Patent 6,284,997 is not required. For a vacuum wall, however, a full welding bead needs to extend along at least one side of the interface between the inclined faces 96 of the staves 90, and the weld must be smooth and clean.

The joining of the staves 90 is simplified if staves 102, illustrated in cross-sectional view of FIG. 10 are machined into generally trapezoidal form but with respective axially extending tongues 104 and grooves 106 are formed in the opposing inclined faces 96. The staves 102 are then assembled by fitting the tongue of one stave 102 into the groove 106 of the neighboring stave 102 with the neighboring inclined faces 106 in abutment. If multiple tongues and grooves are used, the resulting structure has a corrugated joint.

In some applications, it may be desired to form the tube to have a circularized inner surface. In this embodiment, as illustrated in the cross-sectional view of FIG. 11, the joined polygonal tube 100 is machined on its inside, for example on a lathe or reamer, to form a cylindrical inner surface 108 symmetric about the central axis 98. The resulting tube 110 has a circular inner wall 100 and a polygonal outer wall. The interior circular shape greatly simplifies gas flow dynamics during processing of wafers. The outer wall may also be circularized, but this further step is not always necessary.

The tube 100 or 102 may then be stress annealed or have its inner surface bead blasted or otherwise processed to introduce sub-surface damage. Pre-coats of the sort previously described may also be applied.

The silicon parts of the invention are not limited to batch mode thermal CVD reactors. They can be used for plasma CVD and other low temperature processes performed with wafer temperatures below 400°C. For example, a single-wafer plasma CVD reactor has a side wall and a dome onto which the intended deposition material is likely to also be deposited. In the past, the wall and dome have been typically made of quartz, and a plasma

cleaning process has been used to clean the wall and dome surfaces, either between every wafer run or on a less frequent schedule. If the quartz wall, dome, or other part is replaced with a corresponding silicon part surface treated as described above, the plasma cleaning may be eliminated or perhaps delayed until a planned maintenance shutdown. Plasma etching reactors are also subject to deposition of polymeric material and other residues on the chamber walls and parts. The roughened silicon described above will more firmly anchor the residues and reduce the production of particulates.

The invention thus provides a generic approach for reducing particles in substrate processing reactors by the use of surface worked silicon parts. Nonetheless, the silicon material of the parts is readily available at reasonable costs and does not require complex processing.

CLAIMS

1. A method of chemical vapor deposition in a reactor, comprising the steps of:

surface treating a silicon part usable in an interior of a chemical vapor deposition reactor so as to introduce sub-surface damage in said silicon part; and

depositing by chemical vapor deposition a layer of a material onto a wafer in said reactor containing said silicon part.

2. The method of claim 1, wherein said silicon part is a portion of a silicon fixture configured to support a plurality of wafers in said reactor and wherein said depositing step deposits said material onto said plurality of wafers

3. The method of either of claims 1 and 2, further comprising an initial depositing step performed between said surface treating and said depositing steps of depositing by chemical vapor deposition a layer of said material onto said silicon fixture, all slots of said fixtures intended to support wafers during production being vacant during said initial depositing step.

4 The method of any of claims 1 through 3, wherein said material comprises silicon nitride.

5. The method of any of claims 1 through 3, wherein said material comprises polysilicon.

6. The method of any of claims 1 through 5, wherein said silicon part comprises virgin polysilicon.

7. The method of any of claims 1 through 6, wherein said surface treating comprises bead blasting.

8. The method of claim 7, wherein said bead blasting uses particles of silicon

carbide.

9. The method of any of claims 1 through 8, wherein said surface treating produces a surface roughness of at least a portion of said silicon part in a range between 250 and 2500μm Ra.

10. A method of forming a silicon support fixture, comprising the steps of:

fixing together multiple silicon parts together in a configuration capable of supporting a plurality of wafers; and

surface treating said fixed together silicon parts to introduce sub-surface damage in said silicon parts.

11. The method of claim 10, wherein said surface treating includes bead blasting.

12. The method of either of claims 10 and 11, wherein at least some of said silicon parts comprises virgin polysilicon.

13. A silicon support fixture, comprising a plurality of silicon parts fixed together, configured to support a plurality of wafers, and having at least major surface portions with a surface roughness in a range between 0.25 and 2.5μm Ra.

14. The fixture of claim 13, wherein said range extends between 0.5 and 1.9μm Ra.

15. The fixture of claim 14, wherein said range extends between 0.75 and 1.25μm Ra.

16. The support fixture of any of claims 13 through 15, wherein at least some of said silicon parts are composed of virgin polysilicon.

17. A silicon wafer processing reactor for treating a silicon wafer, including:

a processing chamber for a silicon wafer supported therein; and

a part exposed in said chamber composed of silicon and having an exposed surface

portion with a surface roughness in a range between 0.25 and 2.5μm Ra.

18. The reactor of claim 17, wherein said part is a support fixture supporting a plurality of said wafers.

19. The reactor of either of claims 17 and 18, wherein said range extends between 0.50 and 1.9μm Ra.

20. The reactor of claim 19, wherein said range extends between 0.75 and 1.25μm Ra.

21. The reactor of any of claims 12 through 20, wherein at least some of said silicon parts are composed of virgin polysilicon.

22. A circularly symmetric reactor tube formed of substantially pure silicon having an interior bore sized to receive a support fixture capable of holding a plurality of silicon wafers.

23. The reactor tube of claim 22, wherein said bore has a diameter of greater than 200mm.

24. The reactor tube of either of claims 22 and 23, wherein said tube is formed by a wall having a thickness of at least 3mm.

25. The reactor tube of any of claims 22 through 24, further comprising a resistive heater wrapped around said tube.

26. The reactor tube of any of claims 22 through 25, wherein an interior surface of said tube is surface treated to have cracks and pits.

27. The reactor tube of any of claims 22 through 26, wherein said substantially pure silicon is semiconductive silicon.

28. The reactor tube of any of claims 22 through 27, wherein said substantially pure silicon has an impurity atomic fraction for metal of no more than 10^{-6} and for oxygen, carbon, and nitrogen of no more than 10^{-2}.

29. A method of wafer processing, comprising the steps of:

extruding a substantially pure silicon tube;

placing within said tube a support fixture supporting a plurality of silicon wafers; and

heating said tube to thereby thermally process said wafers.

30. The method of claim 29, wherein said tube has a circularly symmetric wall of thickness of at least 3mm.

31. The method of either of claims 29 and 30, wherein said tube has a bore of diameter greater than 200mm.

32. A method of heat treating a silicon wafer, comprising the steps of:

providing a silicon support fixture having support surfaces for supporting at least one silicon wafer and being pre-coated with a layer of silicon nitride;

placing at least one silicon wafer onto said support surfaces of said fixture; and

heating said at one silicon wafer supported on said fixture to a temperature of at least 1320°C.

33. The method of claim 32, wherein said temperature is at least 1350°C.

34. The method of either of claims 32 and 33, wherein said layer of silicon nitride has a thickness of between 0.1 and 10μm.

35. The method of any of claims 32 through 34, where said support fixture is configured to support a plurality of wafers on respective teeth formed in and extending from at least three silicon legs.

36. A method of uniformizing a silicate layer on a substrate, comprising the steps of:

providing a silicon support tower having support surfaces for supporting a plurality of substrates, said tower being pre-coated with a layer of silicon nitride;

placing a plurality of substrates onto support surfaces of said tower, said substrates having a silicate layer coated thereon; and

heating said substrates supported on said tower to an annealing temperature sufficient to reflow said silicate layer.

37. The method of claim 36, wherein said annealing temperature is at least 1200°C.

38. The method of claim 37, wherein said annealing temperature is at least 1350°C.

39. The method of any of claims 36 through 38, wherein said silicate layer is coated by flame hydrolysis.

40. The method of any of claims 36 through 39, wherein said silicon nitride layer is pre-coated by chemical vapor deposition.

41. The method of any of claims 36 through 40, wherein said silicon nitride layer has a thickness of between 0.1 and 10μm.

42. The method of any of claims 36 through 41, wherein said tower has legs including said supporting surfaces formed of virgin polysilicon.

43. The method of any of claims 36 through 42, further comprising surface treating of at least some other portions than said support surfaces of said tower.

44. A tower for supporting a plurality of substrates during processing, comprising:

two silicon bases; and

at least three virgin polysilicon legs attached to said bases and having respective support surfaces for supporting a plurality of substrates and pre-coated with a

layer of a material selected from the group consisting of silicon nitride and polysilicon.

45. The tower of claim 44, wherein said material comprises silicon nitride.

46. The tower of claim 44, wherein said material comprises polysilicon.

47. The tower of any of claims 44 through 46, wherein said there are four of said legs and said support surfaces are disposed at between 68% and 72% of a radius of a circular substrate.

48. The tower of any of claims 44 through 47, wherein said support surfaces are formed in teeth extending at angles of 86° to 89° from longitudinal axes of said legs.

49. The tower of any of claims 44 through 48, wherein said legs are surface treated to introduce sub-surface damage prior to being pre-coated with said layer.

50. The tower of any of claims 44 through 49, wherein said a layer has a thickness of between 0.1 and 10μm.

51. A method of forming a silicon tube, comprising: fixing together a plurality of at least twenty of silicon staves all extending parallel to a central axis.

52. The method of claim 51, wherein said fixing process includes welding.

53. The method of claim 51, wherein said fixing process includes applying a silica-based spin-on glass to interfaces between said staves.

54. The method of any of claims 51 through 53, wherein said staves have grooves and tongues fittable in said grooves and extending parallel to said central axis.

55. The method of any of claims 51 through 54, wherein said staves are arranged in

a circular pattern about said central axis.

56. The method of any of claims 51 through 55, wherein staves comprise virgin polysilicon.

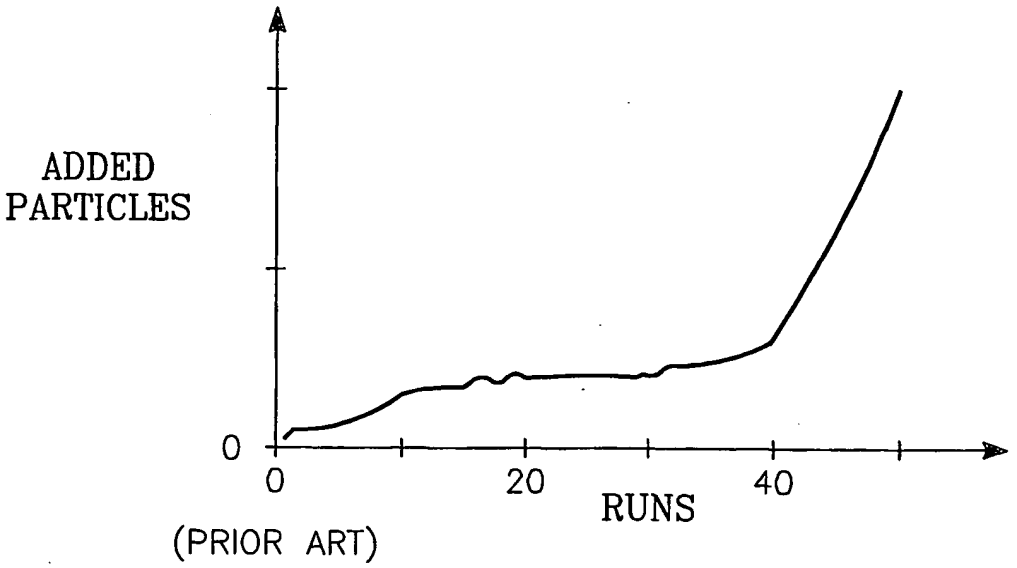
57. The method of any of claims 51 through 56, wherein said staves have trapezoidal shapes.

58. The method of any of claims 51 through 57, further comprising circularizing an interior surfaces of said staves fixed together.

59. A silicon tube, comprising a plurality of at least twenty of silicon staves fixed together in a closed pattern with an interior bore and extending parallel to a central axis.

60. The silicon tube of claim 59, wherein said staves are composed of virgin polysilicon.

61. The silicon tube of either of claims 28 and 29, wherein said staves are welded together.



(PRIOR ART)

FIG. 1

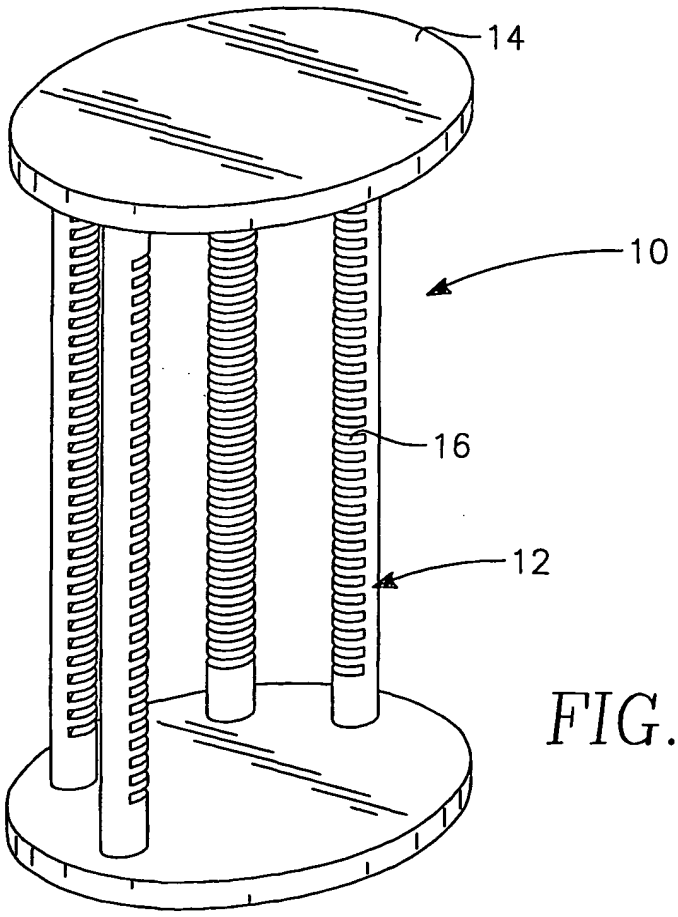


FIG. 2

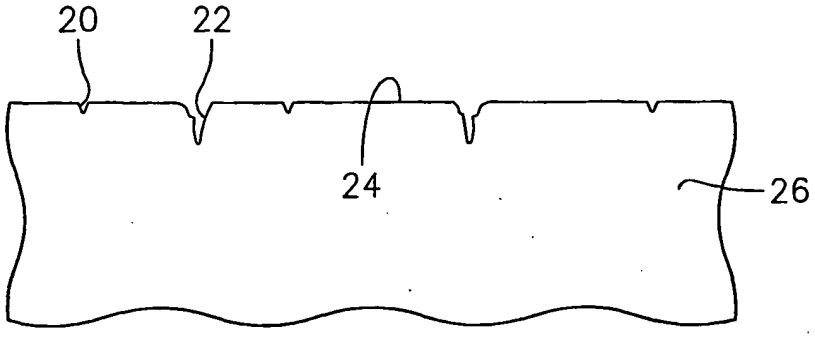


FIG. 3

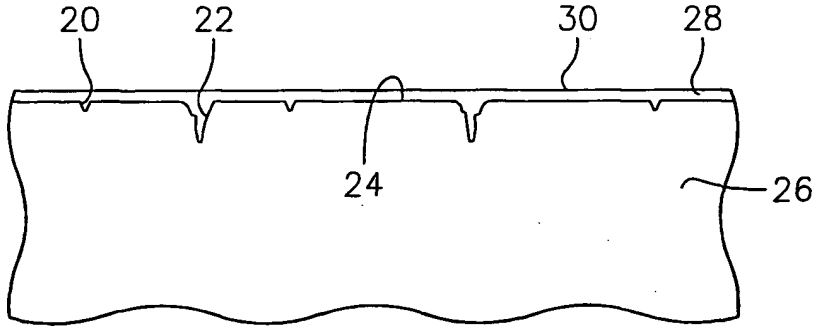


FIG. 4

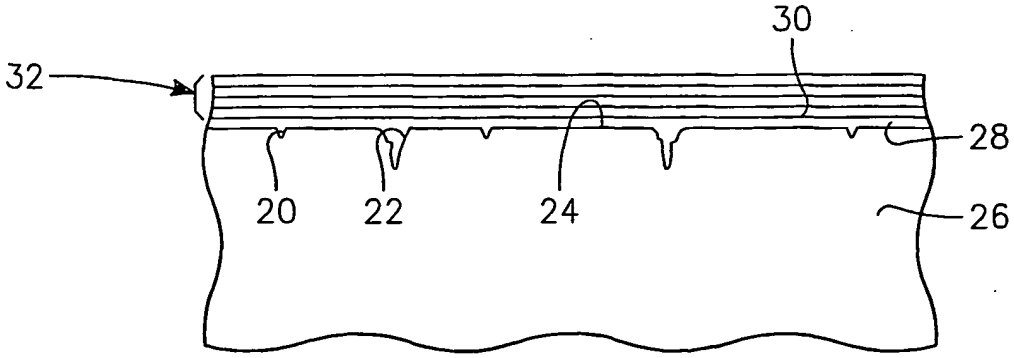


FIG. 5

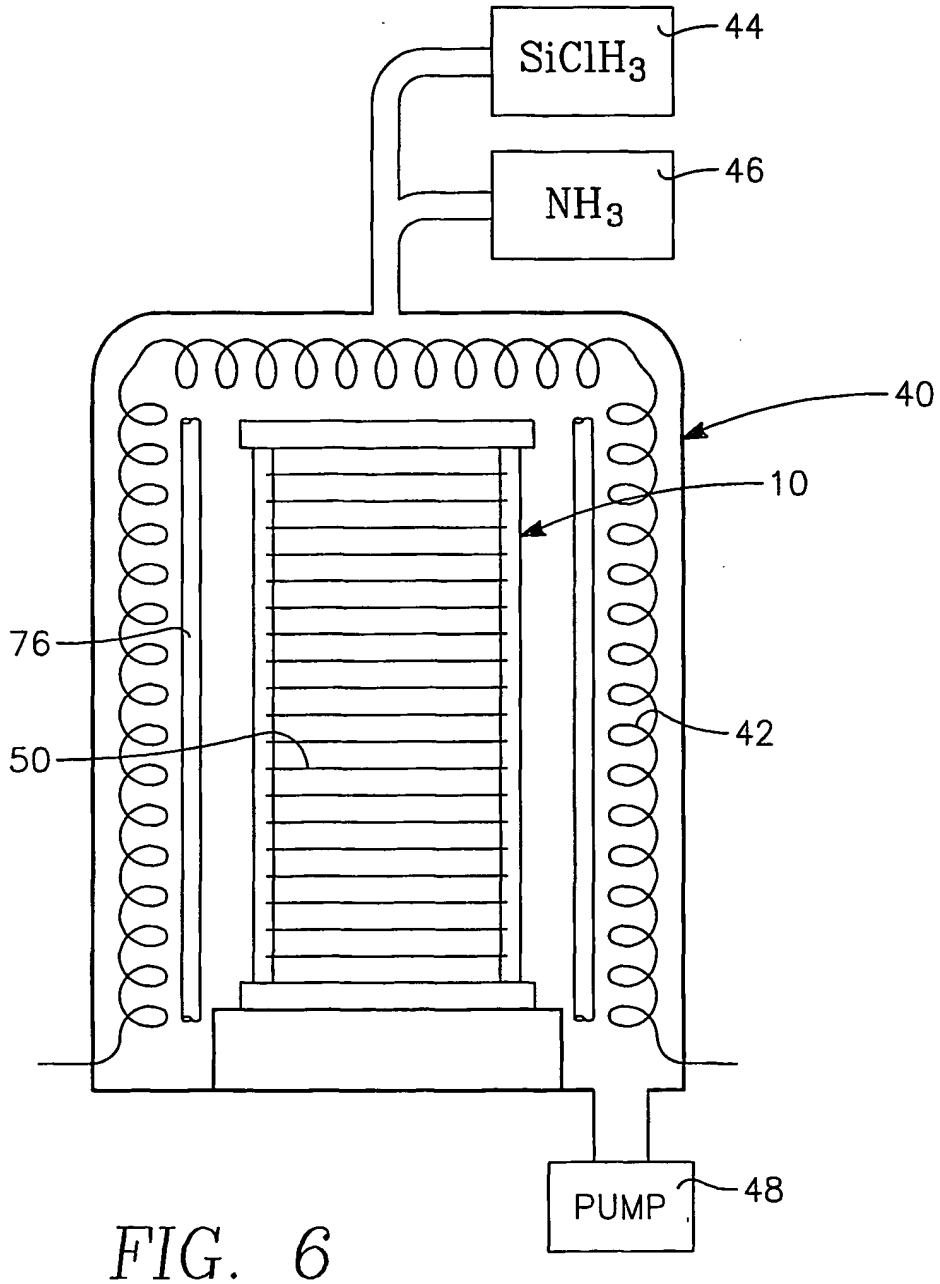


FIG. 6

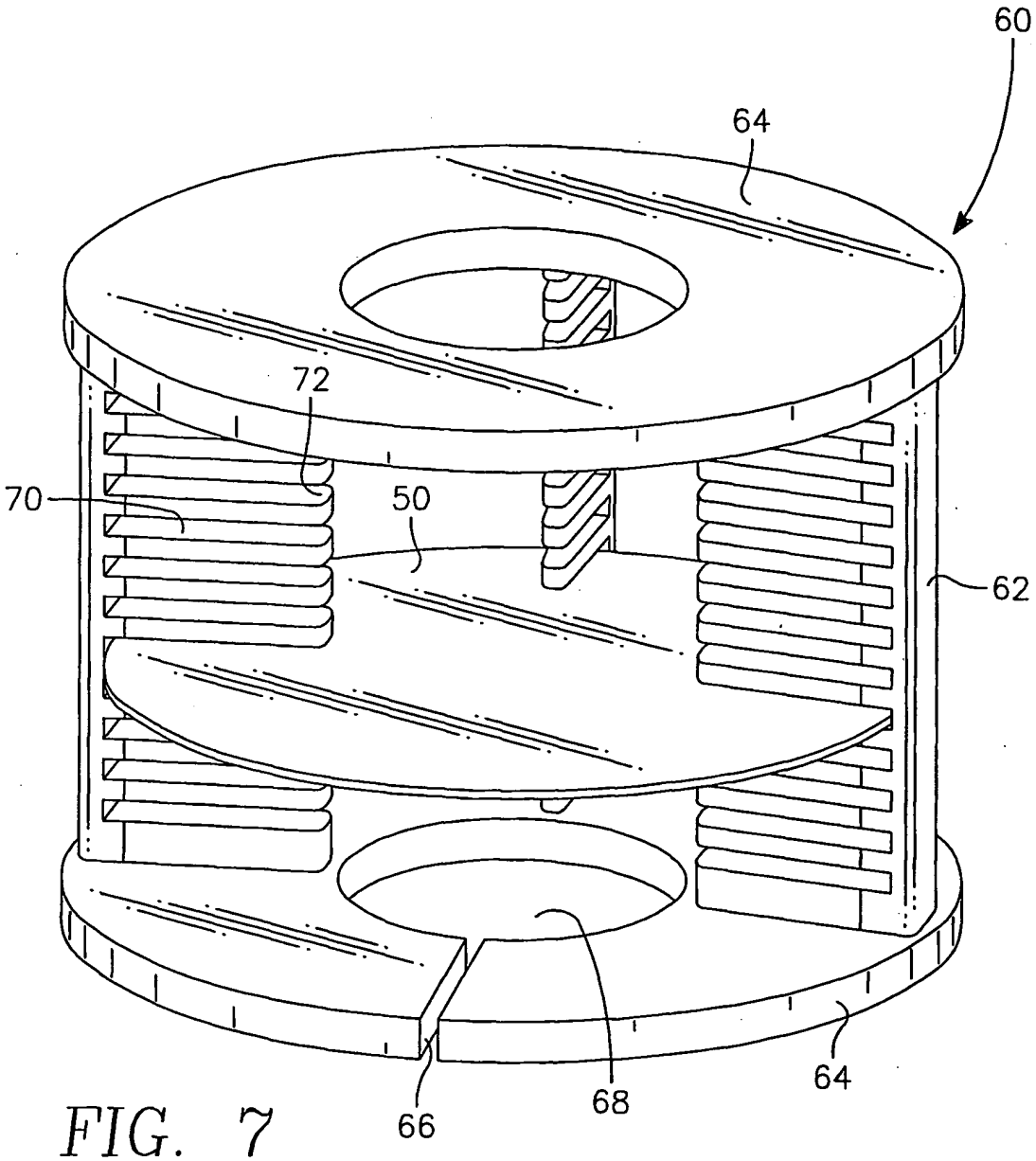


FIG. 7

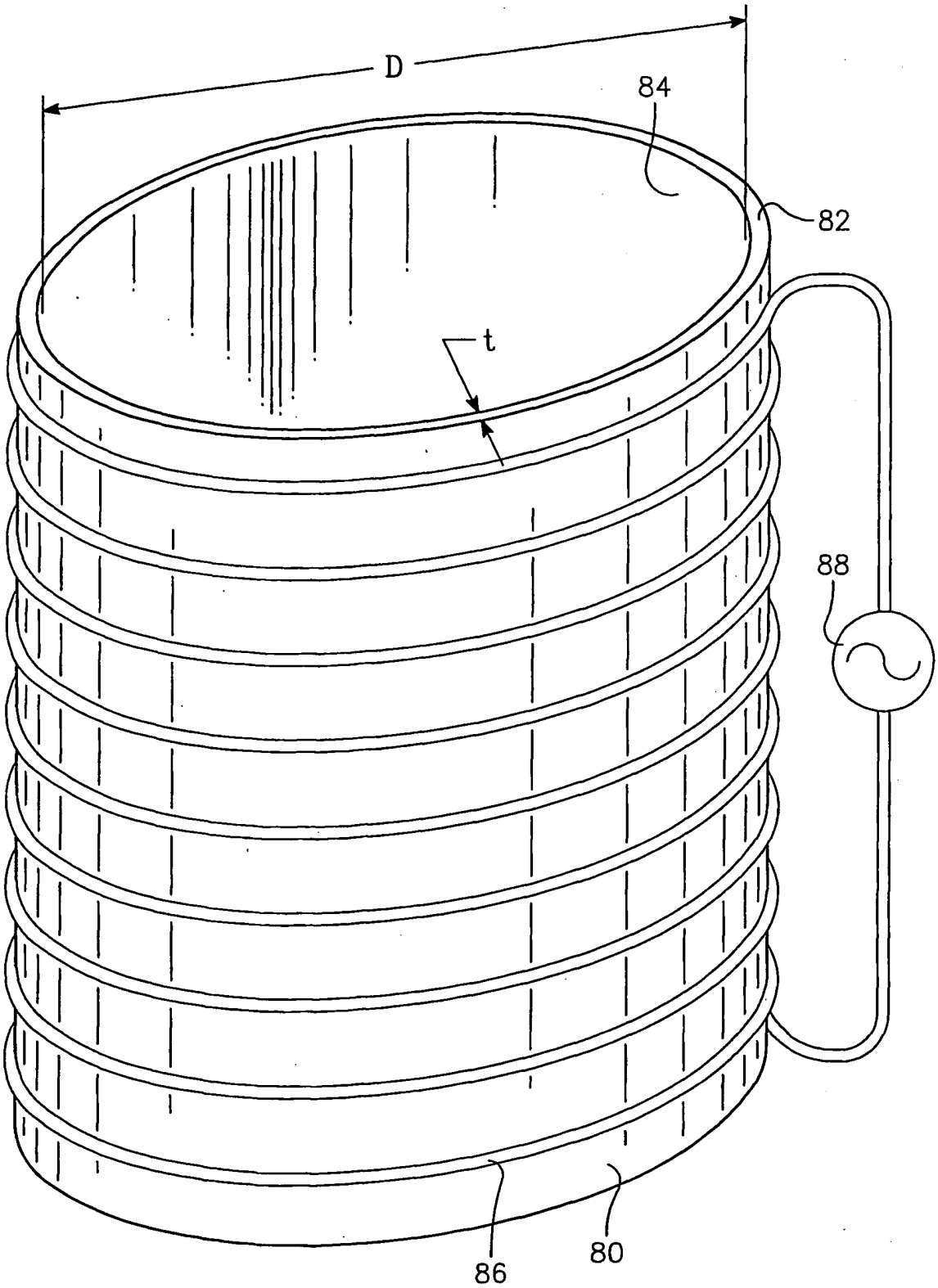


FIG. 8

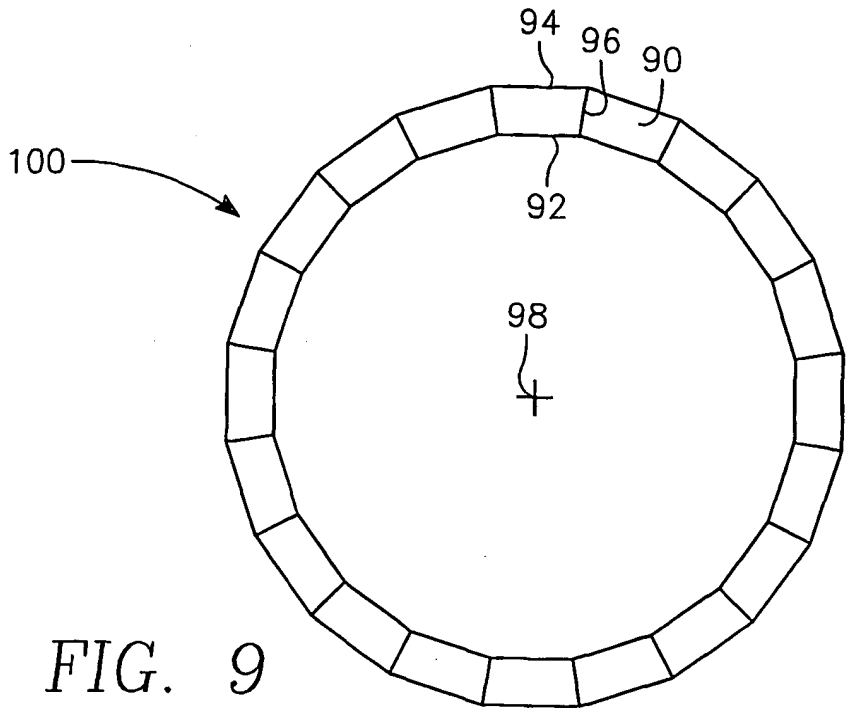


FIG. 9

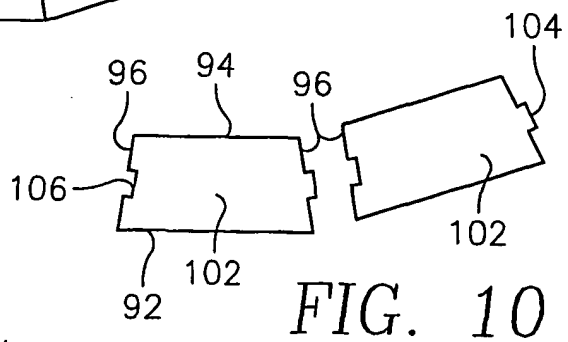


FIG. 10

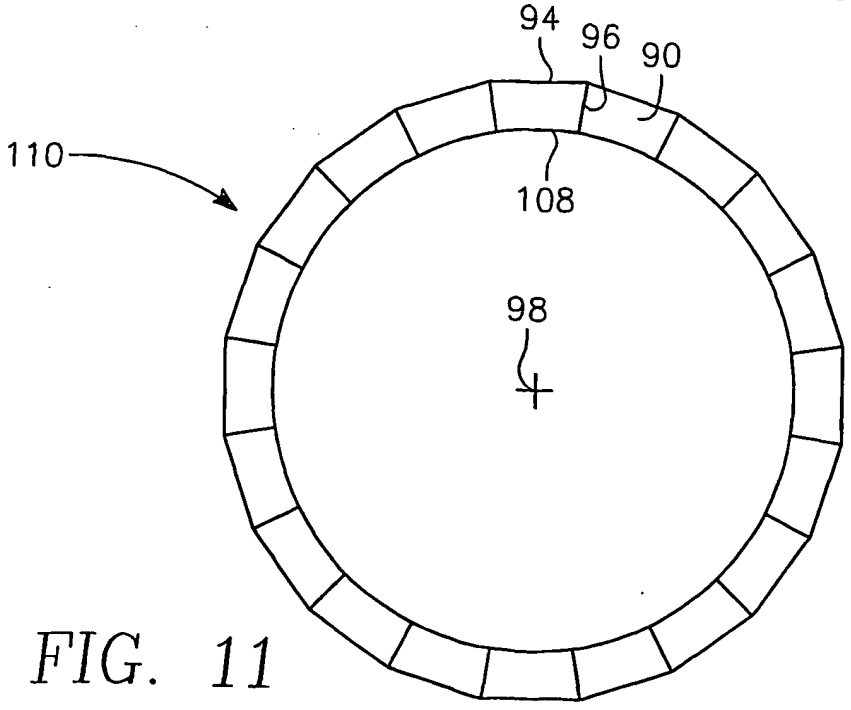


FIG. 11